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EXAMINER	
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ART UNIT	PAPER NUMBER
2187	

NOTIFICATION DATE	DELIVERY MODE
12/17/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/535,591	VAN DE WAERDT ET AL.	
	Examiner	Art Unit	
	Gary W. Cygiel	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 4-8, 10-14, 16-18 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Sherwood et al. (NPL:Predictor-Directed Stream Buffers) (hereinafter referred to as Sherwood).

Consider **Claim 1**,

Sherwood teaches a method of data retrieval comprising the steps of:

providing a first memory circuit (Sherwood:Fig 3);

providing a stride prediction table (SPT) that is indexed with cache line miss information (Sherwood:Fig 3, Sec 4.2, load-PC (for a missed load) is used to index into the stride table. Page 9:Left Column:Lines 1-3,only cache block addresses are used.);

providing cache memory circuit (Sherwood:Fig 3);

executing instructions for accessing data within the first memory (Instructions must be executed to access data within the first memory.);

detecting a cache miss (Sherwood:Sec 4.3 ¶3, detects two cache misses in a row); and

only allowing accesses to the SPT in response to a detection of a cache miss (Sherwood:Sec 4.2/4.3, the load-PC (for a missed load) is used to index into the stride table.);and

only allowing updates to the SPT in response to the detection of a cache miss. (Sherwood:Sec 4.2/4.3, prediction table is *only* updated on a cache miss (Sec 4.2 ¶2)).

Consider **Claims 2 and 16**,

Sherwood further teaches wherein the cache memory circuit is a stream buffer (Sherwood:Fig 3).

Consider **Claim 4**,

Sherwood further teaches wherein the cache memory circuit and the SPT are within a same physical memory space (Sherwood:Fig 3).

Consider **Claim 5**,

Sherwood further teaches wherein the first memory is an external memory circuit separate from a processor executing the instructions (Sherwood:Fig 3,data line from/to next lower level of memory.).

Consider **Claims 6 and 7**,

Sherwood further teaches wherein the step of detecting a cache miss includes the steps of:

determining whether an instruction to be executed by the processor is a memory access instruction;

when the instruction is a memory access instruction, determining whether data at a memory location of the memory access instruction is present within the cache; and,

when the data is other than present within the cache, detecting a cache miss, and accessing and updating the SPT only when the cache miss has occurred (Sherwood:Sec 4.3 ¶3, a cache miss occurs when a requested memory line is not in the cache, therefore requiring the first two limitations of these claims.).

Consider **Claim 8**,

Sherwood further teaches wherein the step of allowing access provides a step of filtering that prevents unnecessary access and updates to entries within the SPT (Sherwood:Sec 4.3).

Consider **Claim 10**,

Sherwood further teaches wherein the SPT comprises an address field, and where a size of the address field is less than an address space used to index the SPT (Sherwood:Sec 4.2 ¶3, SPT stores the last address for the load. Page 9:Left Column:Lines 1-3,only cache block addresses are used and *not* the full address.).

Consider **Claim 11**,

Sherwood teaches an apparatus comprising:

a stride prediction table (SPT) that is indexed with cache line miss information (Sherwood:Fig 3, Sec 4.2, load-PC (for a missed load) is used to index into the stride table. Page 9:Left Column:Lines 1-3,only cache block addresses are used.); and

a filter circuit for use with the SPT, the filter circuit preventing both accesses and updates to the SPT unless a cache miss is detected (Sherwood:Sec 4.2/4.3, the load-PC (for a missed load) is used to index into the stride table; prediction table is *only* updated on a cache miss (Sec 4.2 ¶2.).

Consider **Claim 12**,

Sherwood further teaches a memory circuit, the memory circuit for storing the SPT therein (Sherwood:Fig 3).

Consider **Claim 13**,

Sherwood further teaches a cache memory, the cache memory residing within the memory circuit (Sherwood:Fig 3).

Consider **Claim 14**,

Sherwood further teaches wherein the memory circuit is a single ported memory circuit (Sherwood:Fig 3, Page 5, paragraph labeled prediction, only one request can be processed at a time.)

Consider **Claim 17**,

Sherwood teaches a method of data retrieval comprising the steps of:

providing a first memory circuit (Sherwood:Fig 3);

providing a stride prediction table (SPT) that is indexed with cache line miss information (Sherwood:Fig 3, Sec 4.2, load-PC (for a missed load) is used to index into the stride table. Page 9:Left Column:Lines 1-3,only cache block addresses are used.);

providing cache memory circuit (Sherwood:Fig 3);

executing instructions for accessing data within the first memory (Instructions must be executed to access data within the first memory.);

detecting a cache miss (Sherwood:Sec 4.3 ¶3, detects two cache misses in a row); and

restricting accesses to the SPT in response to the detection of a cache miss (Sherwood:Sec 4.2/4.3; the load-PC (for a missed load) is used to index into the stride table, prediction table is *only* updated on a cache miss (Sec 4.2 ¶2)).

Consider **Claim 18**,

Sherwood further teaches wherein the step of restricting provides a step of filtering that prevents unnecessary access and updates to entries within the SPT (Sherwood:Sec 4.2/4.3).

Consider **Claim 20**,

Sherwood further teaches wherein the SPT comprises an address field, and where a size of the address field is less than an address space used to index the SPT (Sherwood:Sec 4.2 ¶3, SPT stores the last address for the load. Page 9:Left Column:Lines 1-3,only cache block addresses are used and *not* the full address.).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 3, 9, 15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sherwood et al. (NPL:Predictor-Directed Stream Buffers) (hereinafter referred to as Sherwood) in view of Handy (NPL: the Cache Memory book) (hereinafter referred to as Handy).

Consider **Claim 3, 9, 15 and 19**,

Sherwood teaches a method according to claim 1 or 13 respectively, but does not specifically disclose all the details regarding the circuits construction.

Handy does teach these limitations such as:

wherein the cache memory circuit is a random access cache memory (Handy:Page 28, SRAM cell used in internal cache.).

wherein the cache memory circuit is integral with the processor executing the instructions (Handy:Page 28, CPU on same chip as on-chip cache.).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to implement the circuit construction concepts as taught by Handy in the system of Sherwood because they are notoriously well known concepts in the art. The use of these methods constitutes only design choice and has no novelty in the art.

6. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sherwood et al. (NPL:Predictor-Directed Stream Buffers) (hereinafter referred to as Sherwood) in view of Matas et al. (NPL:Memory 1997).

Consider **Claim 21**,

Sherwood teaches a method of data retrieval, the method comprising:

providing a first memory circuit (Sherwood:Figure 3);

providing a memory having a cache memory circuit and a stride prediction table (Sherwood:Figure 3) that is indexed with cache line miss information (Sherwood:Fig 3, Sec. 4.2, load-PC (for a missed load) is used to index into the stride table. Page 9:Left Column:Lines 1-3, only cache block addresses are used);

in a filter circuit,

receiving an application stream having a plurality of access instructions for accessing data in the first memory circuit (Sherwood:Page 8, Table 2; Page 9:Left Column, describes various programs (application streams)).

for each of the plurality of access instructions that are load access instructions,

accessing the cache memory to determine whether data at a memory location of the load access instruction is present within the cache (Sherwood:Page 5:section 4.2, determining if instruction hit or missed in cache.), and

when the data is other than present within the cache, detecting a cache miss for the load access instruction (Sherwood:Page 6:Sec. 4.3, detects two cache misses in a row.),

restricting accesses and updates to the SPT to only load memory access instructions for which a cache miss is detected (Sherwood:Sections 4.2/4.3, load-PC (for a missed load) is used to index into the stride table; prediction table is *only* updated on a cache miss (Sec 4.2 ¶2).);

in response to an update to the SPT indicative of one of said detected cache misses, executing instructions to access the SPT and predict a cache miss (Sherwood:Section 4.3, allocates a stream buffer in response to two cache misses. Sec 3.3.2 describes stream buffer operation.); and

in response to a predicted cache miss, control the loading of a stream cache based upon the memory location of the load access instruction (Sherwood:Sections 4.2/4.3, stride based buffer allocation. Sec 3.3.2 describes stream buffer operation.).

Sherwood fails to expressly describe the use of a single-ported SRAM for the cache memory circuit and stride prediction table. However, Matas et al. does describe the use of SRAM for cache memory applications. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use single-port SRAM (Matas:Fig. 8-6/8-7) for the cache memory circuit and stride prediction table of Sherwood because single-port SRAM is commonly used in cache applications and is faster and uses less power than other types of memories (Matas:Page 8-1 ¶1).

Response to Arguments

7. Applicant's arguments filed 23 November 2010 have been fully considered but they are not persuasive.

[A] Re: Stride prediction table is only accessed in response to a cache miss.

The applicant argues that there is no disclosure in Sherwood of a stride prediction table (SPT) which is only accessed in response to a cache miss

(REMARKS:Page 6:Lines 17-20). There are several specific arguments which will be addressed separately below.

[A1] Re: REMARKS: Page 6, Line 11 – Page 6, Line 24

The applicant argues that the rejections provided by the examiner "do not assert explicit correspondence to limitations directed to limiting all accesses to a SPT by 'only allowing accesses to the SPT in response to the detection of a cache miss.'" However, the rejections are supported with clarifying comments when a citation alone may be unclear.

[A2] Re: REMARKS: Page 6, Line 24 – Page 7, Line 17

The applicant correctly notes that it is the stride table that is updated upon a miss, but continues by stating there is no teaching which restricts all access to the asserted prediction table which the applicant claims is the Markov Predictor shown in Figure 3. However, the Markov Predictor is not just a separate structure from the Stride Predictor (Sherwood:Figure 3), but also use a fundamentally different method of operation. Markov predictors are based on the probability of state transitions (Sherwood:Page 2 §2.2) instead of a history based stride (Sherwood:Page 2 §2.1). The Markov Predictor of Sherwood:Figure 3 *is not* the claimed Stride Prediction Table for at least the reasons provided above.

Since the Markov Table *is not* the SPT as asserted by the applicant (REMARKS:Page 7:Lines 7/8) the frequency of access or updates to the Markov Table are unrelated to the claimed SPT access controls related to a cache miss.

[A3] Re: REMARKS: Page 7, Line 18 – Page 8, Line 6

The applicant argues that a review of the Sherwood reference "teaches that its SPT is accessed once 'each cycle…to make a prediction.'" This is completely incorrect as the entire content of the portion of Sherwood, from which the applicant is quoting, states that "[e]ach cycle, one stream buffer is chosen to make a prediction using the address predictor, according to priority heuristics described in Section 4.4." (Sherwood:Page 5:Left Column:Lines 17-19). The quote the applicant has provided has absolutely nothing to do an SPT, or the Stride-Filtered Markov Predictor which is the basis of the art rejections.

The applicant continues to rely on Figure 2 and §4.1 of Sherwood to support their argument that Sherwood fails to teach restricting access to an SPT. The applicant responded to the examiners assertion that the system of Fig 2(§4.1) is related, but different to the system of Fig 3(§4.2) by writing that it was "clearly in error, as the cited system in Figure 3 operates in the same manner." The applicant attempts to support this argument by referring to the discussion of §4.2 "which indicates that the stride table includes both a last and current address and the stride is calculated by 'current miss address – last address.'" This appears to support the examiners assertion that the systems are related, but different since there is no disclosure of a stride table in the description of the generic system of §4.1.

The applicant describes that "[t]his (non-miss) access appears necessary to the Sherwood reference's purpose as directed to using this difference calculation to store 'only the cache misses' in the Markov table (the difference is not stored when the 'last address' is not a cache miss)." However, the applicant

fails to detail the cause of this non-miss access. The applicant may be referring to the updating of the Markov table described in Sherwood §4.2 beginning at ¶3. However, as noted in **[A]** above, the Markov Table *is not* the claimed Stride Prediction Table and the claims do not address non-miss access to elements other than the SPT.

[B] Re: REMARKS: Page 8, Line 7 – Page 8, Line 24

The applicant argues (REMARKS:Page 8:Lines 14/15) that "the Office Action has not established correspondence to a filter circuit that restricts accesses and updates to a SPT" as described in Claim 21. Although the examiner has provided clarifying comments describing the content in the cited sections that is relevant to the claimed limitation, as evidenced by the current and previous office action, the applicant further requests that the examiner do "more than generally citing four columns of the Sherwood reference" (REMARKS:Page 8:Line 18). Since the examiner has already performed the requested task in the current and previous office actions, the level of detail the applicant requires is not clear. It appears in this case that the applicant is uncertain with regards to a physical structure of the filter circuit. Since Claim 21 is a method claim, the filter circuit structure is the elements or group of elements which perform the methods of the claimed filter circuit.

[C] Re: REMARKS: Page 8, Line 25 – Page 9, Line 11

The applicant argues that the examiner "fails to establish that the Sherwood reference necessarily detects a cache miss as claimed" (REMARKS:Page 9:Lines 29/30). The applicant continues by asserting that "[a]s

is well known, a cache miss can be detected in a number of ways" and lists type of memory accesses that may result in a cache miss, but fails to disclose a single one of the well-known ways in which a cache miss can be detected that does not involve the steps cited by the examiner as being inherent. The following is repeated from the previous office action for convenience:

The applicant argues that the following steps of Claims 6 and 7 are not necessarily present in the Sherwood reference:

determining whether an instruction to be executed by the processor is a memory access instruction; and

when the instruction is a memory access instruction, determining whether data at a memory location of the memory access instruction is present within the cache.

Sherwood describes that "In the write-back stage, the load instruction is checked to see if it hit or missed in the L1 data cache." This *requires* determining whether data at a memory location of the memory access instruction is present within the cache. An attempt to access the cache *is* the result of determining that an instruction to be executed by the processor is a memory access instruction.

The applicant argues that there may be other ways to detect a cache miss, but fails to provide an example of how this can be accomplished without some determination that the instruction is a memory access instruction and further determining whether the data is in the cache. Cache miss information cannot "simply be provided" or provided "based upon functionality that happens

after a cache miss" without the above steps because without the above steps cache miss information simply does not exist.

[D] Re: REMARKS: Page 9, Line 12 – Page 10, Line 9

The applicant argues that “the Office Action has failed to establish correspondence as the rejection provides no explanation as to how the SRAM in the Matas reference would be combined with the memory in the Sherwood reference, as to where the Matas reference discloses a "single- ported" SRAM, or any rationale for the specific modification of the Sherwood reference as proposed.” With respect to where the Matas reference discloses a single-ported SRAM, the examiner cited specific figures. A person of ordinary skill in the art at the time of the invention would recognize the cited diagrams (Matas:Figures 8-6/8-7) as being single ported SRAM cells. In regards to how the SRAM of Matas would be combined and the motivation for doing so, these were clearly provided in the previous rejection. The applicant states that “the asserted rationale for combining the references (that SRAM is “commonly used” and is “faster and uses less power”) is devoid of any explanation relevant to the specific modification at hand” (REMARKS:Page 19:Lines 3-6). However, arguments of counsel cannot take the place of factually supported objective evidence. See, e.g., In re Huang, 100 F.3d 135, 139-40, 40 USPQ2d 1685, 1689 (Fed. Cir. 1996); In re De Blauwe, 736 F.2d 699, 705, 222 USPQ 191, 196 (Fed. Cir. 1984).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

[A] Hong, Byung Il (US PGPub No. 2005/0026084) – contains figures that show the difference between a single port SRAM (Figure 1) and dual port SRAM (Figure 2) memory cell.

[B] Joseph et al. (NPL: Prefetching using Markov Predictors) – describes the operation of a Markov Predictor.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary W. Cygiel whose telephone number is

(571)270-1170. The examiner can normally be reached on Tuesdays and Thursdays 12:00pm-2:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Ellis can be reached on (571)272-4205. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Gary W Cygiel
Examiner
Art Unit 2187

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